NR

Code No: A7008, A5703

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.Tech I Semester Examinations, March/April-2011

VHDL MODELING OF DIGITAL SYSTEMS

(COMMON TO ELECTRONICS AND COMMUNICATION ENGINEERING, VLSI SYSTEM DESIGN)

Time: 3hours **Max. Marks: 60**

Answer any five questions

All questions carry equal marks

\- - -

1. Explain about the following giving examples:
   a) Hardware Simulation.
   b) Oblivious Simulation.
   c) Event Driver Simulation. [12]

2. Explain about a VHDL based design process with examples. [12]

3. a) Draw the circuit and explain about VHDL implementation of sequence detector.
   b) Explain about timing and concurrency in VHDL programming. [6+6]

4. a) Write a procedure in VHDL for converting integers between 0 and 255 to a byte.
   b) Write a data flow description for a full adder in VHDL. [6+6]

5. a) Using 4 n sec and 8 n sec delays for the NOR and XOR logic gates respectively, write VHDL descriptions for a two input gates. Use single delay nodes.
   b) Using only nand 2 and nand 3 descriptions, write VHDL descriptions for a D- latch. [6+6]

6. a) Write an entity declaration and an average delay architecture for an Exclusive-OR gate with a tphe of 10 n.sec and tphe of 8 n. sec.
   b) Show the gate level implementation of master-slave JK Flip Flop in VHDL. [6+6]

7. Describe an 8-bit shift register in VHDL using guarded block statements. The structure has a serial input for right shifting the data and a single serial output. All activities are to be synchronized with the leaching edge of the clock. [12]

8. Write notes on any **TWO**:
   a) Data flow description test bench for the par wan CPU.
   b) Three state Browsing.
   c) Predefined and user defined attributes. [12]

*****